

FIG. 1

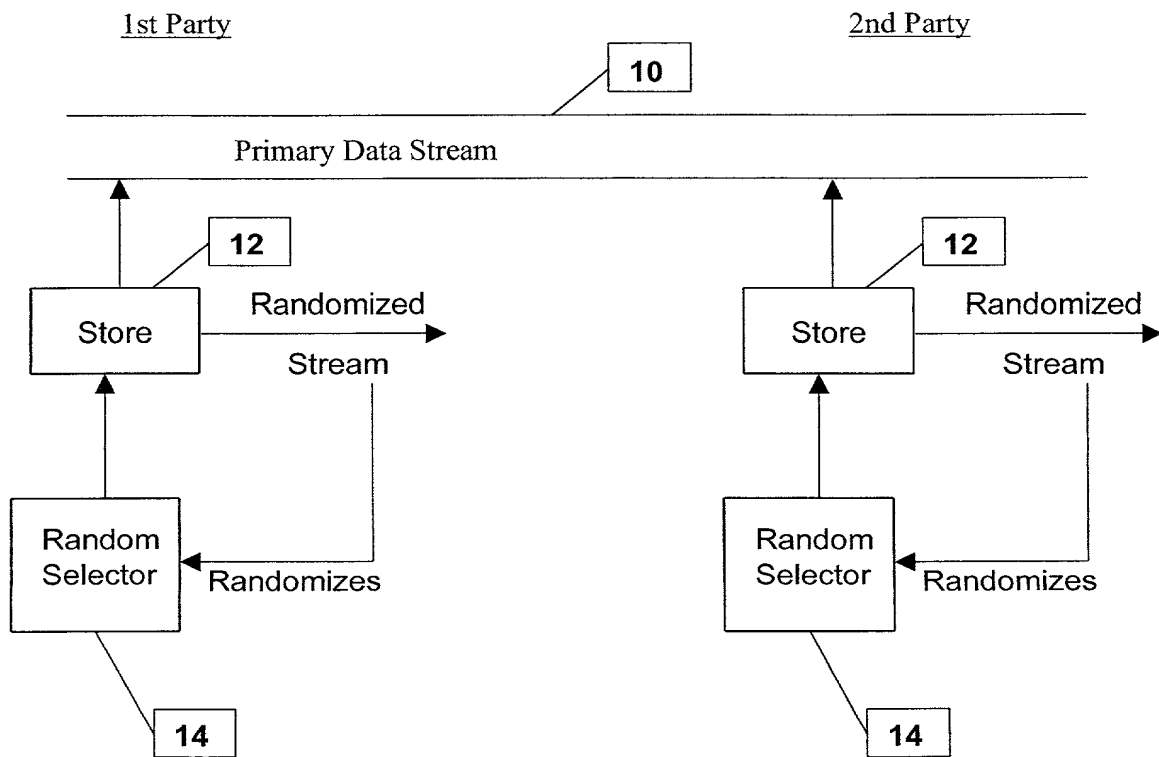


FIG. 2

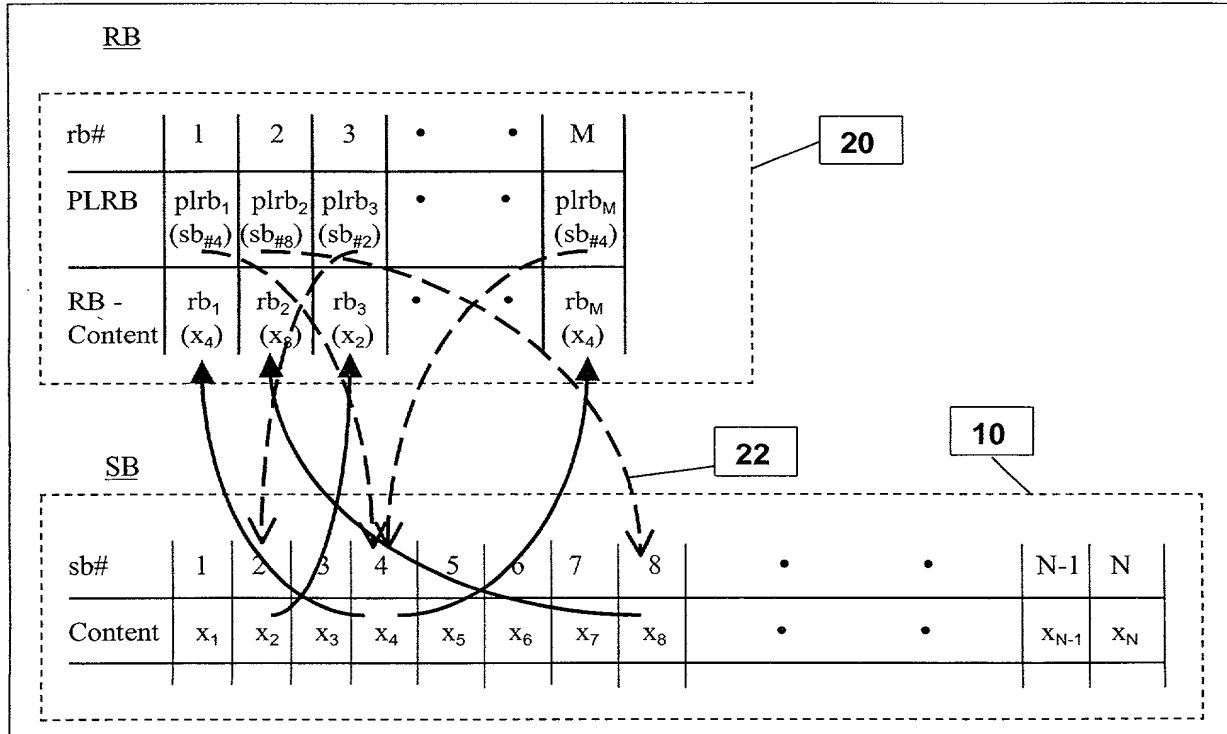
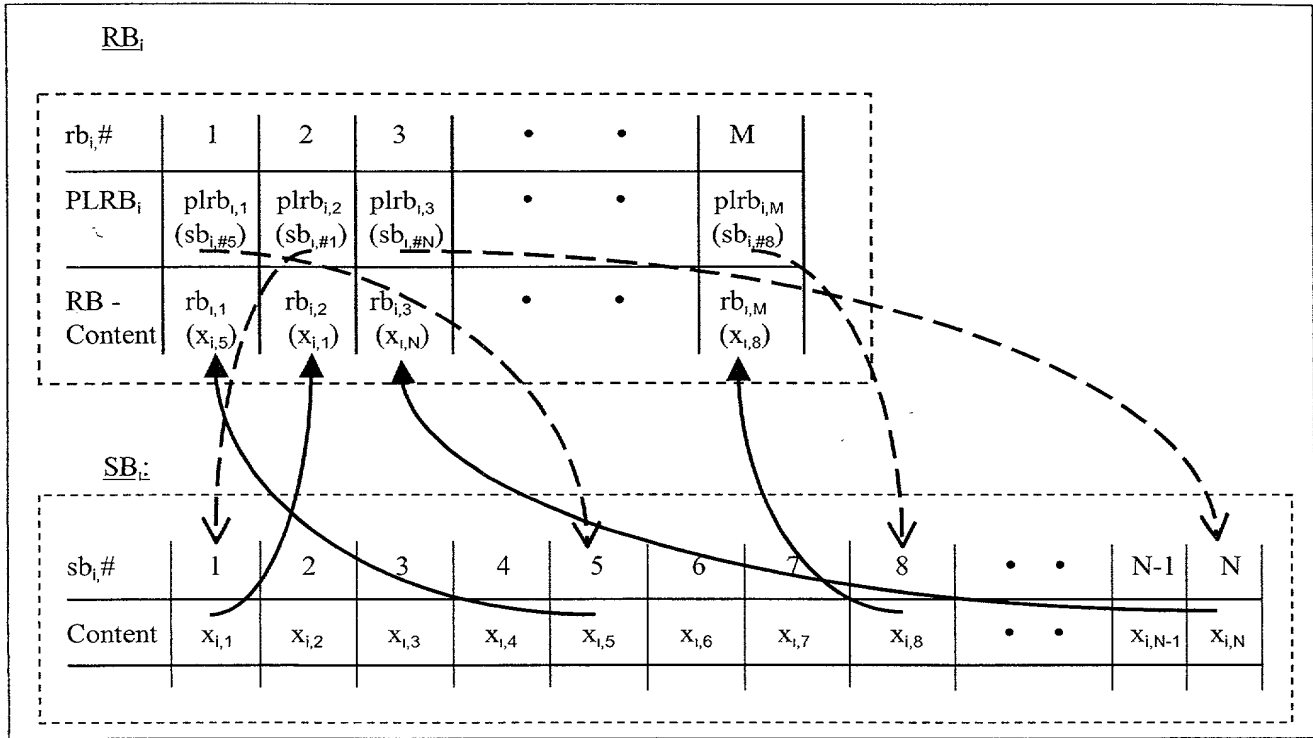


FIG. 3

RndPro_i



RndPro_{i+1}

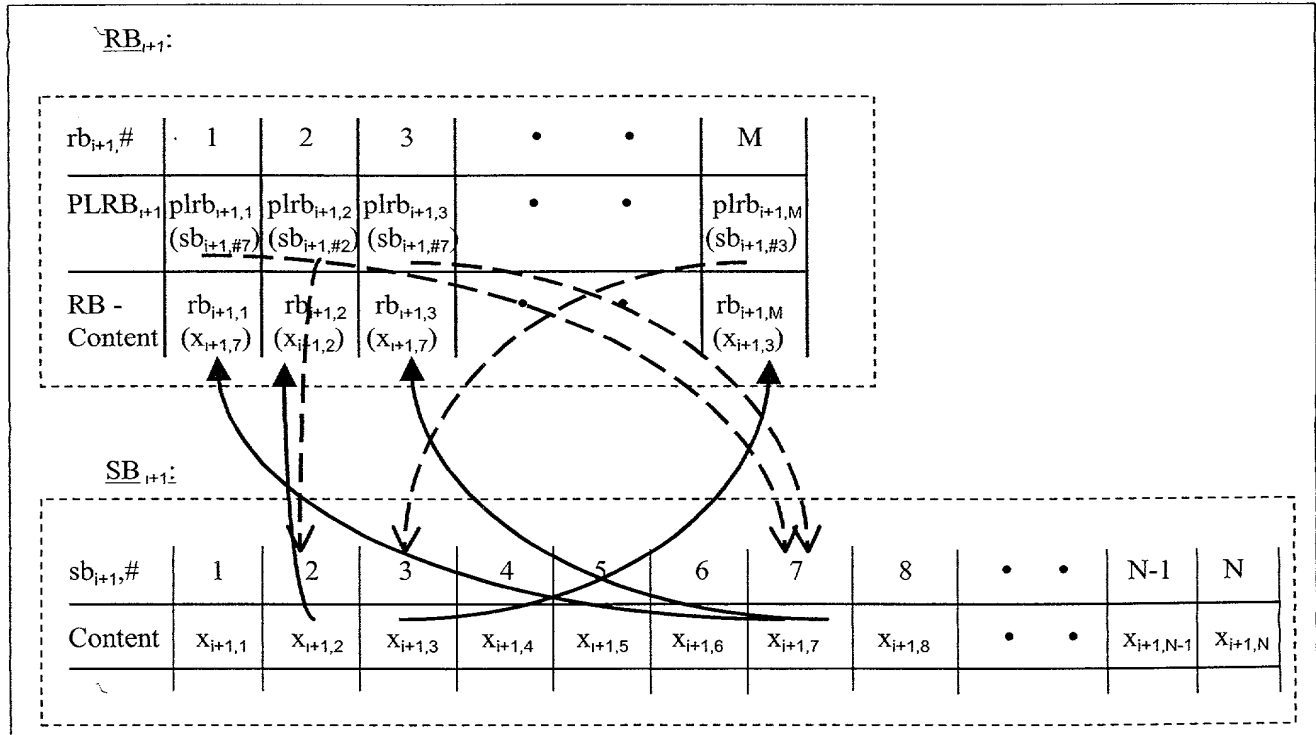


FIG. 4

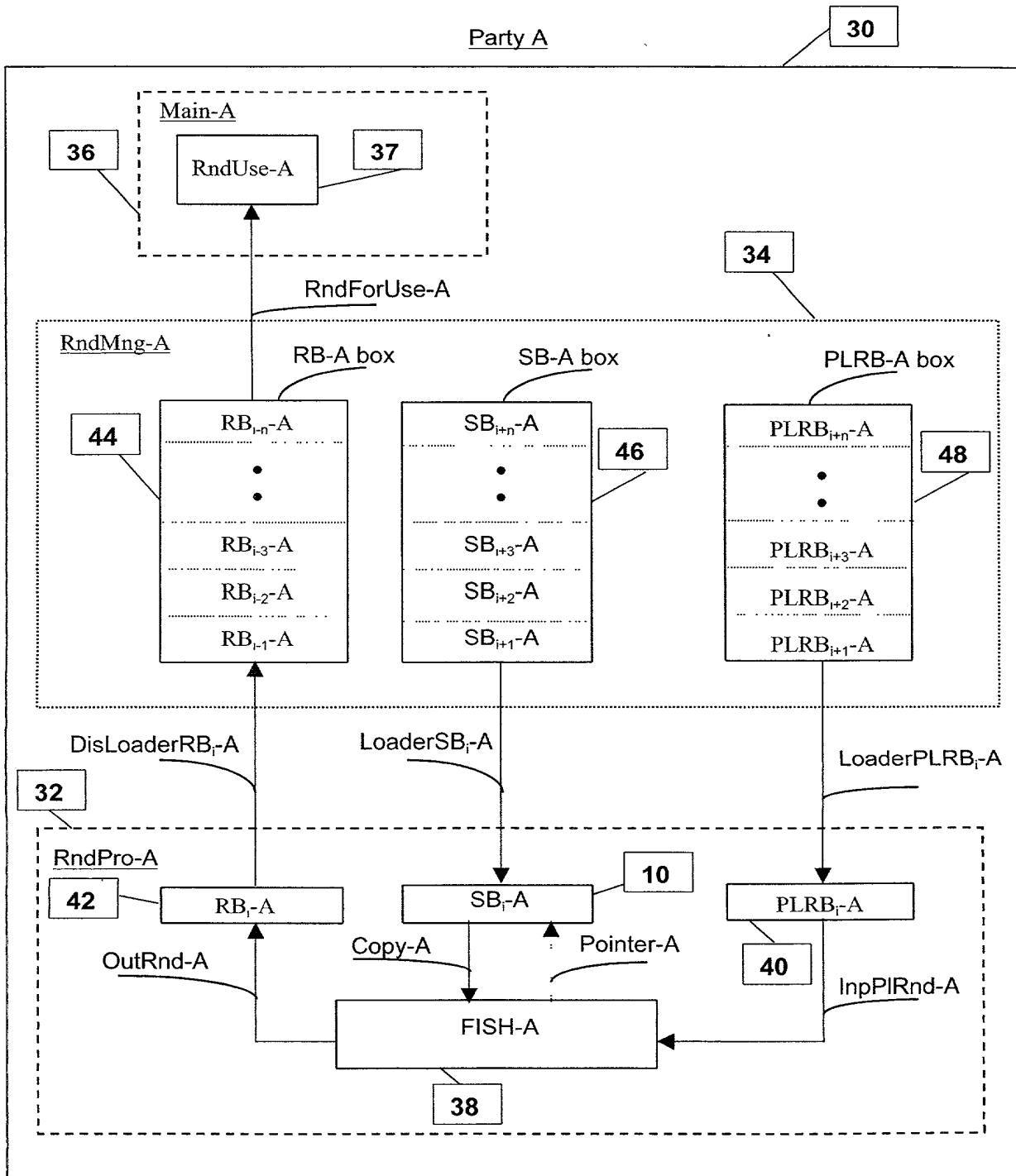


FIG. 5

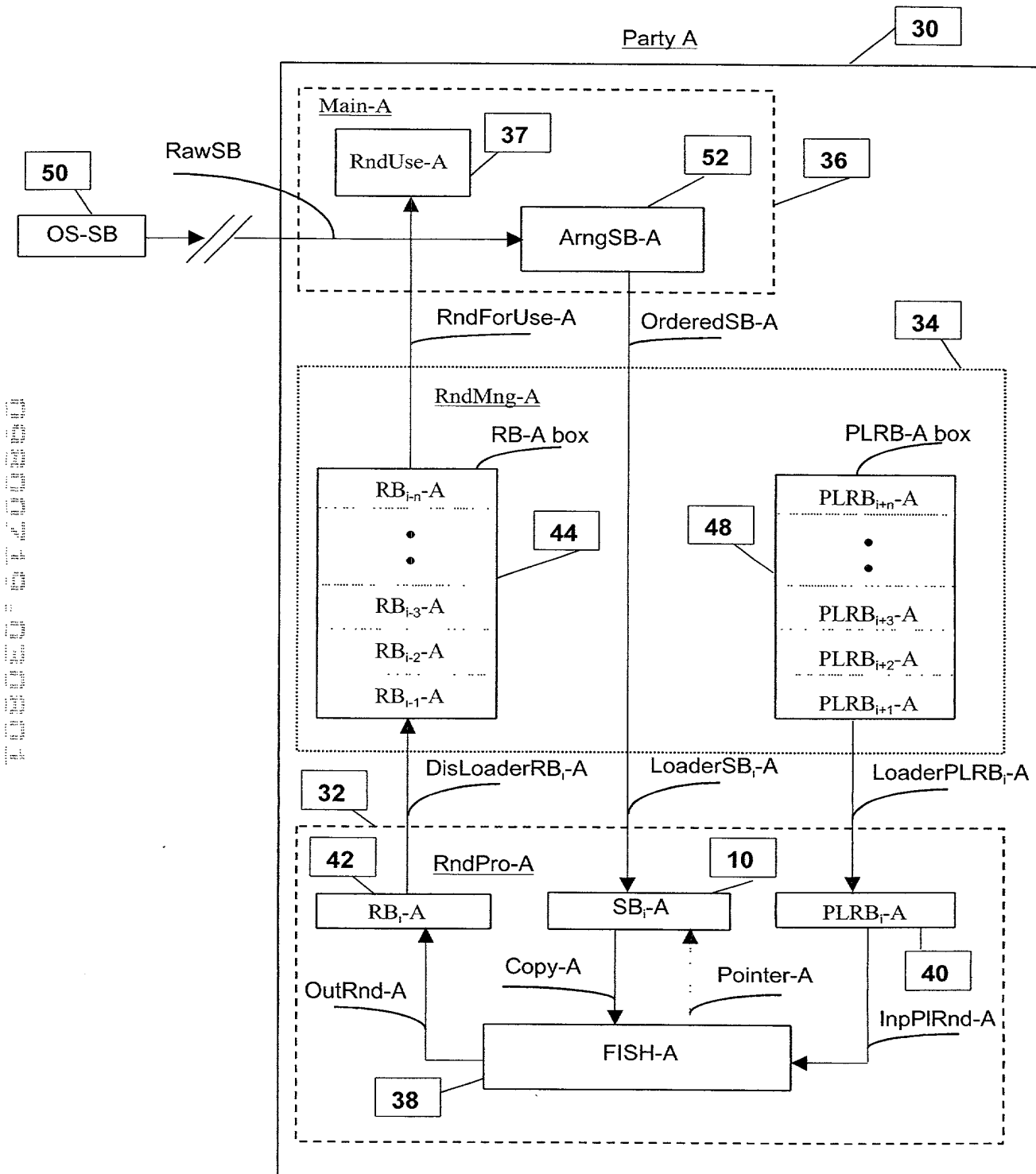


FIG. 6

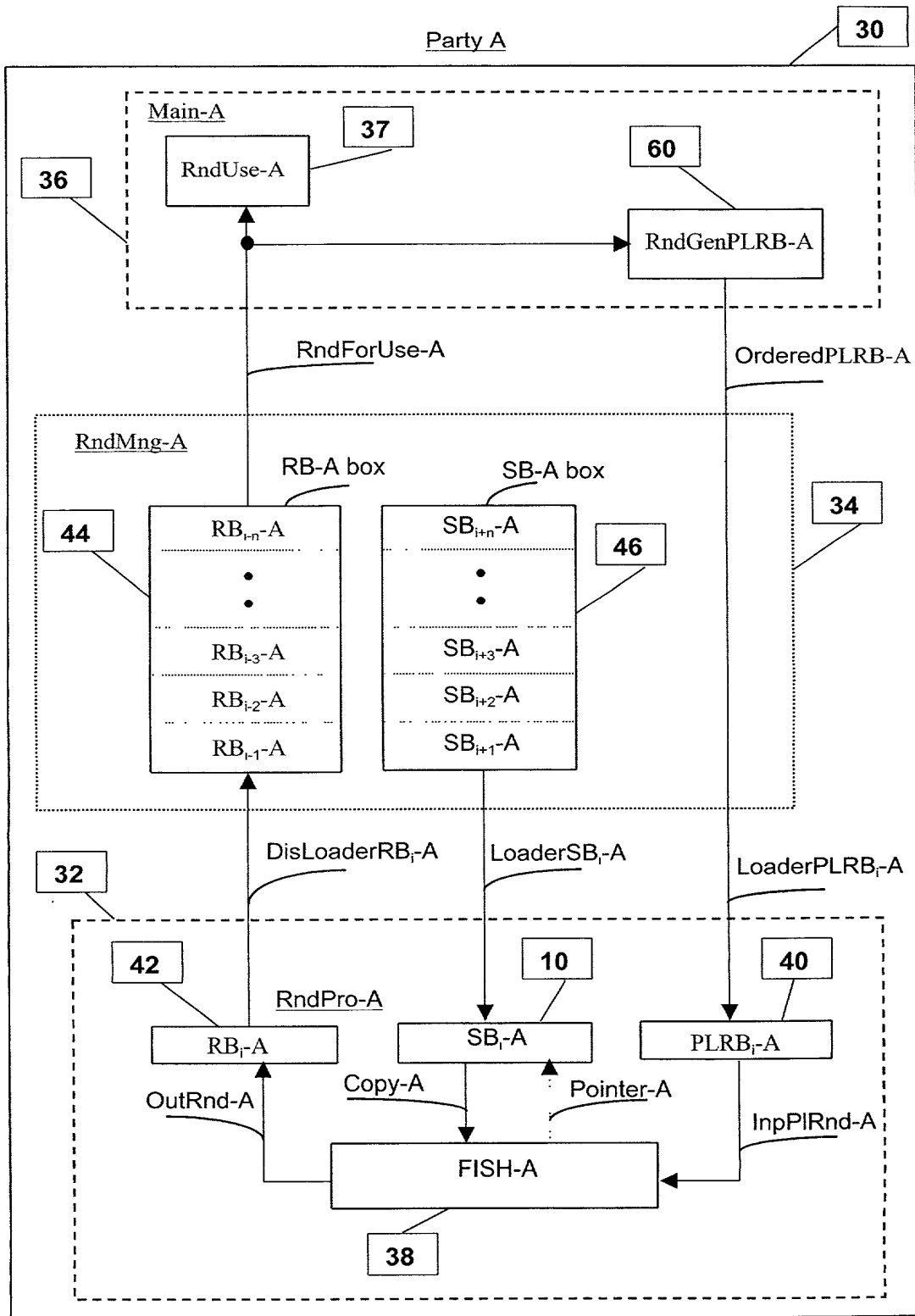


FIG. 7

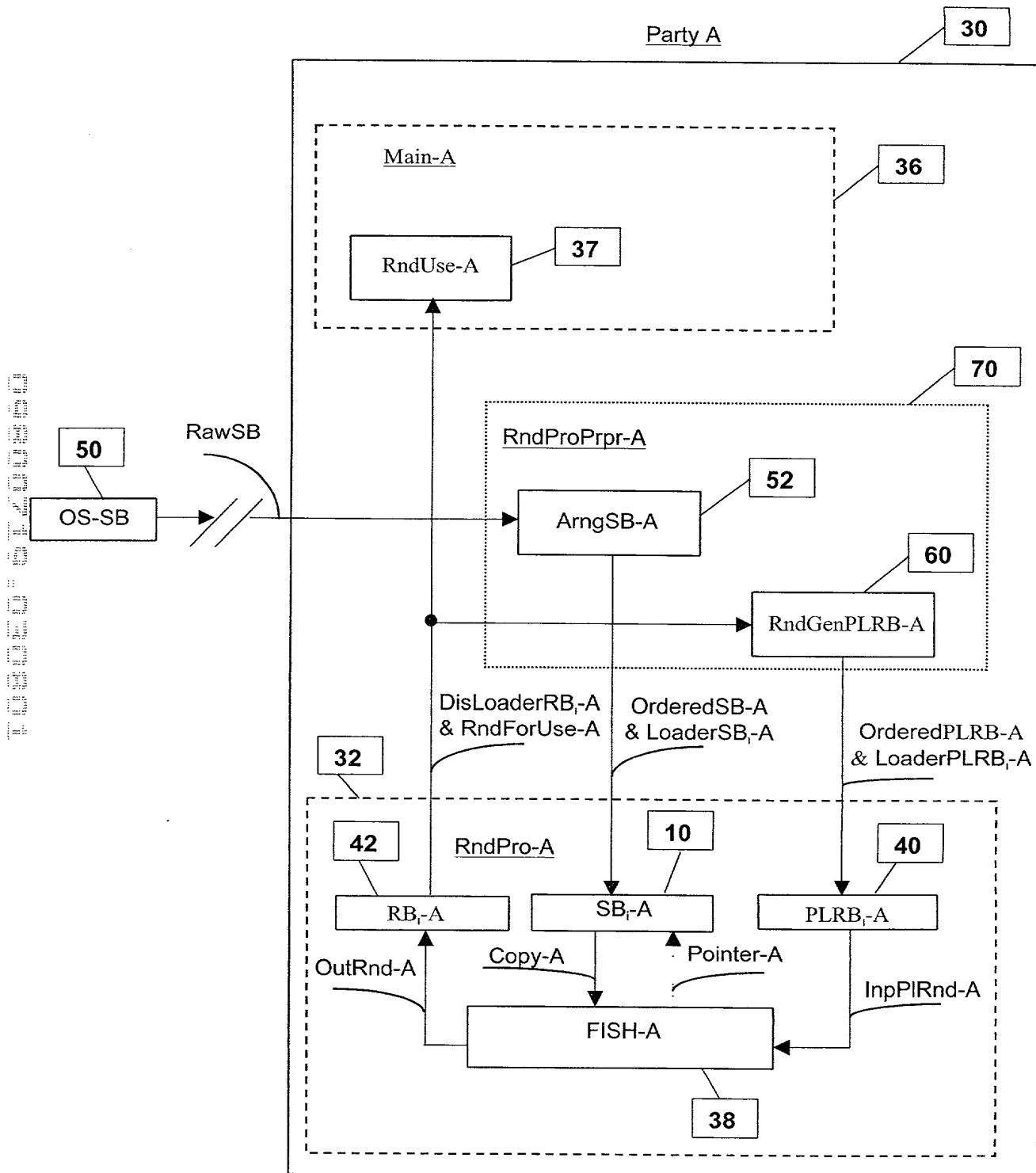


FIG. 8

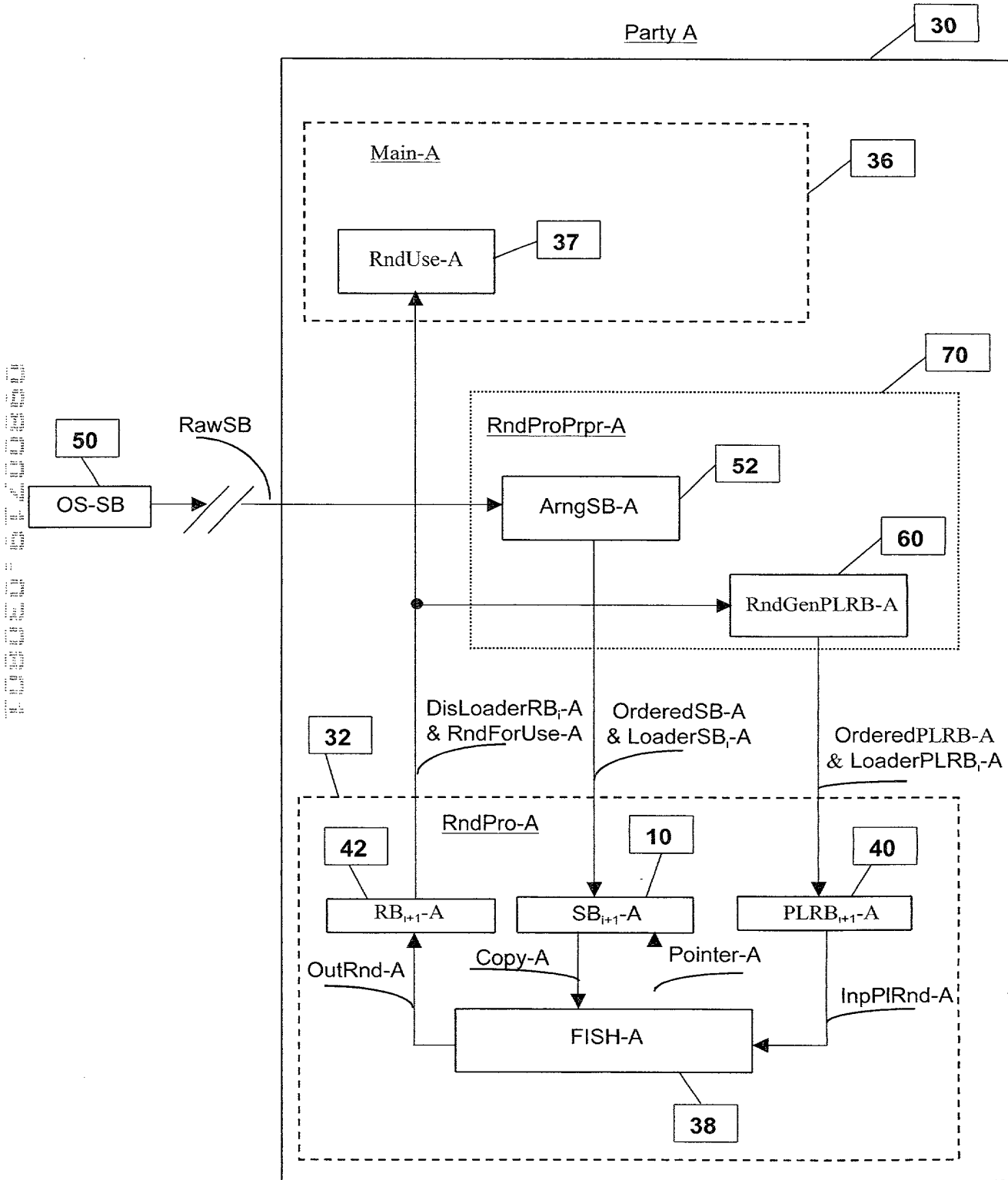


FIG. 9

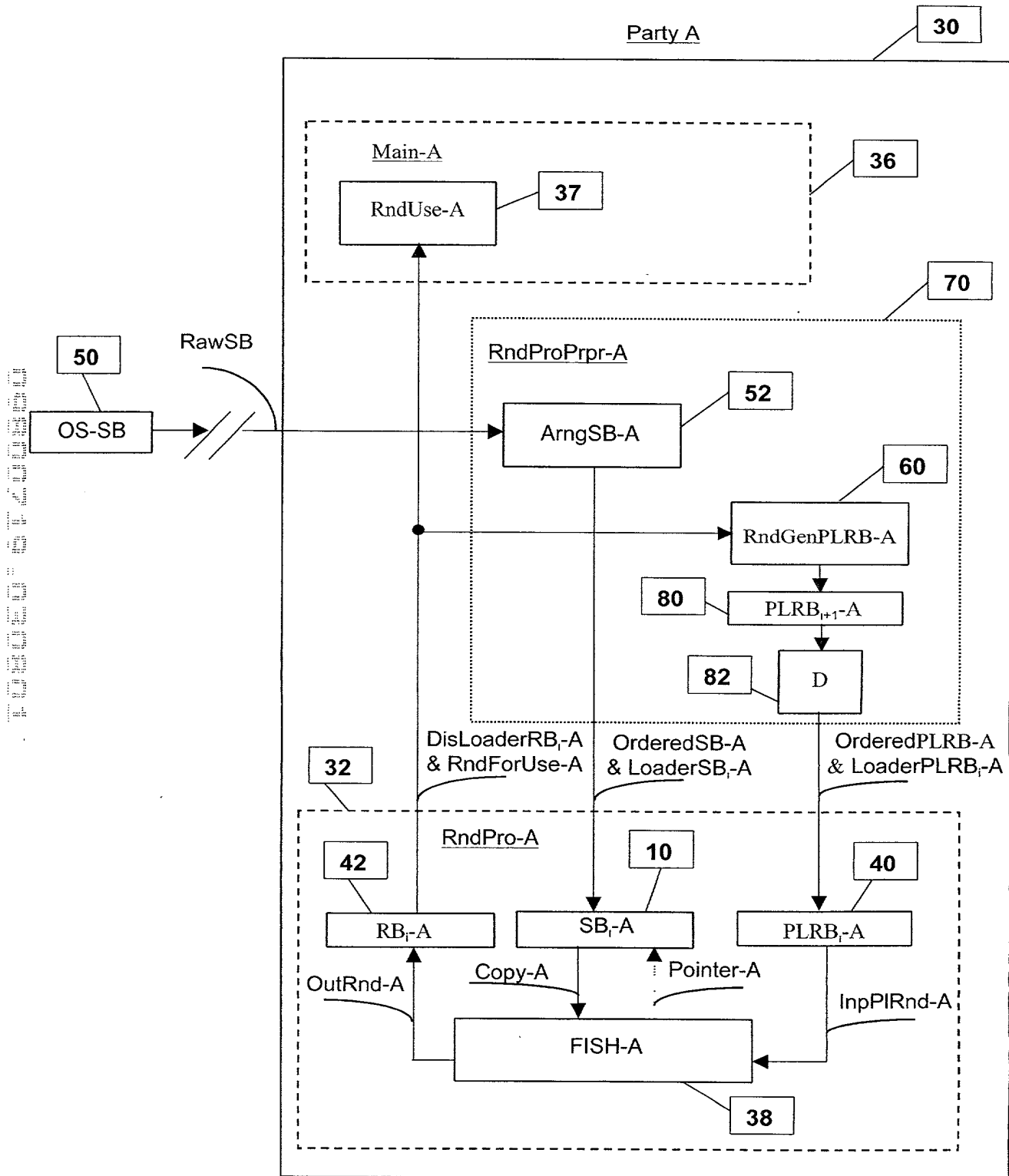


FIG. 10

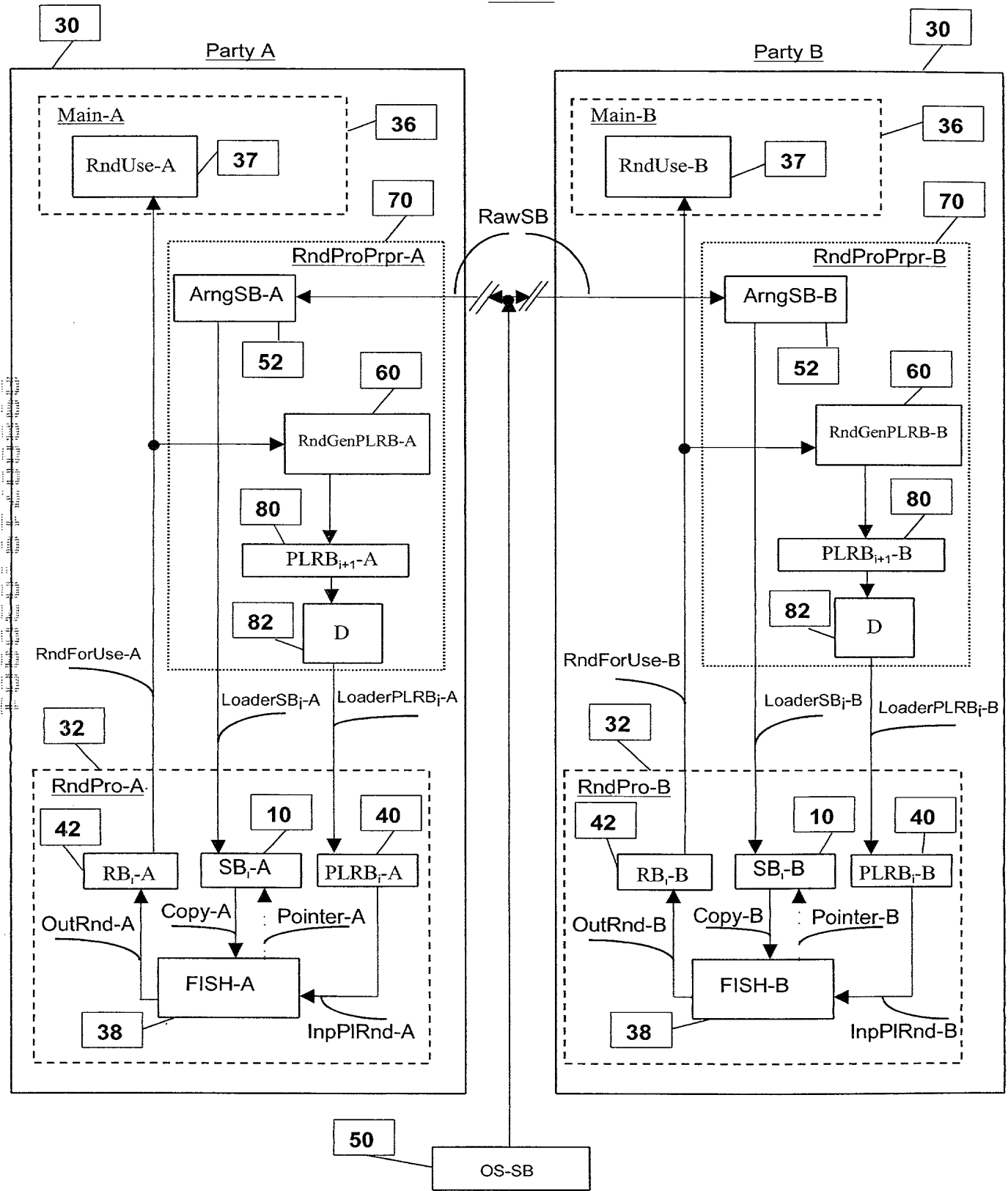


FIG. 11

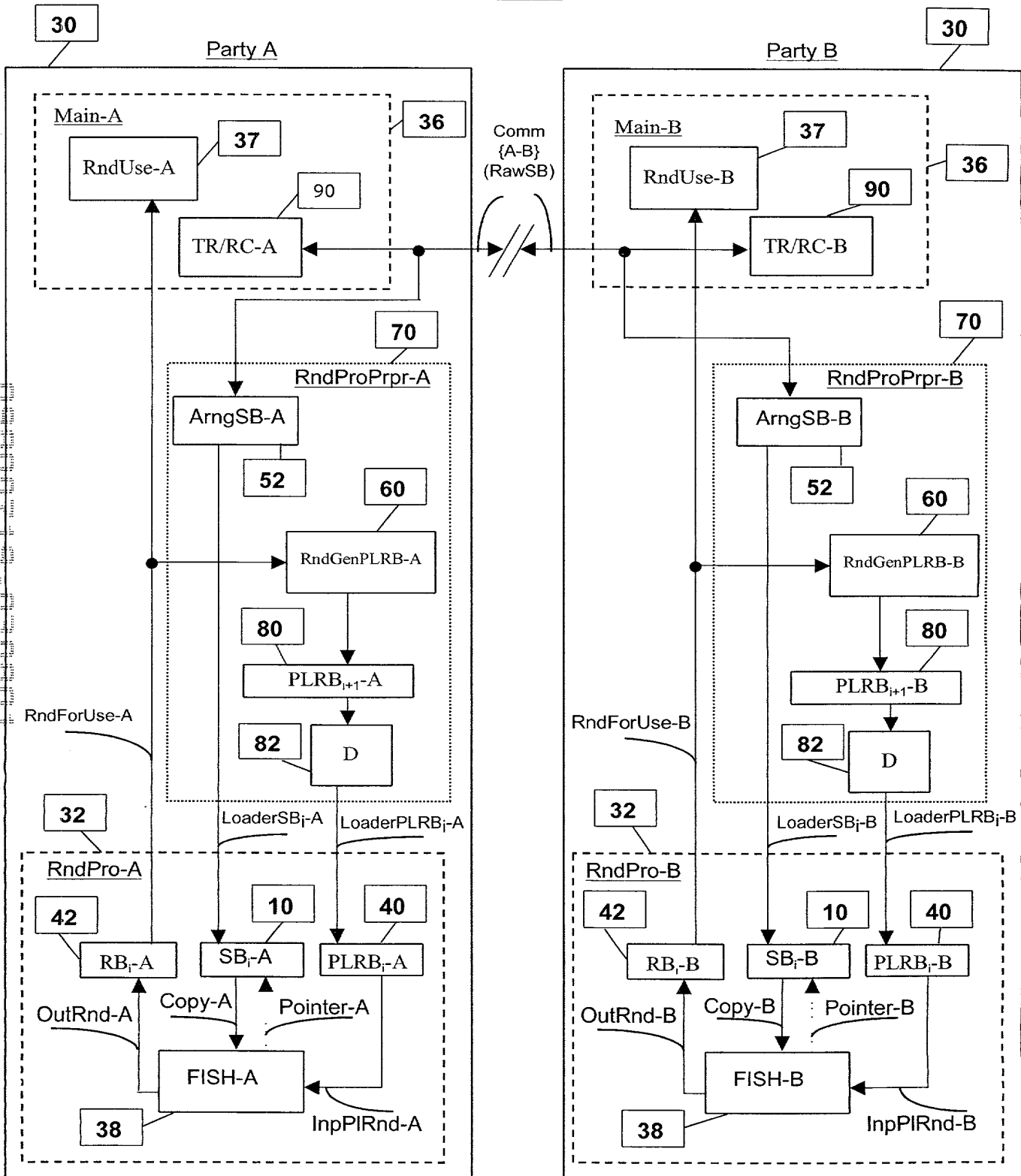


FIG. 12

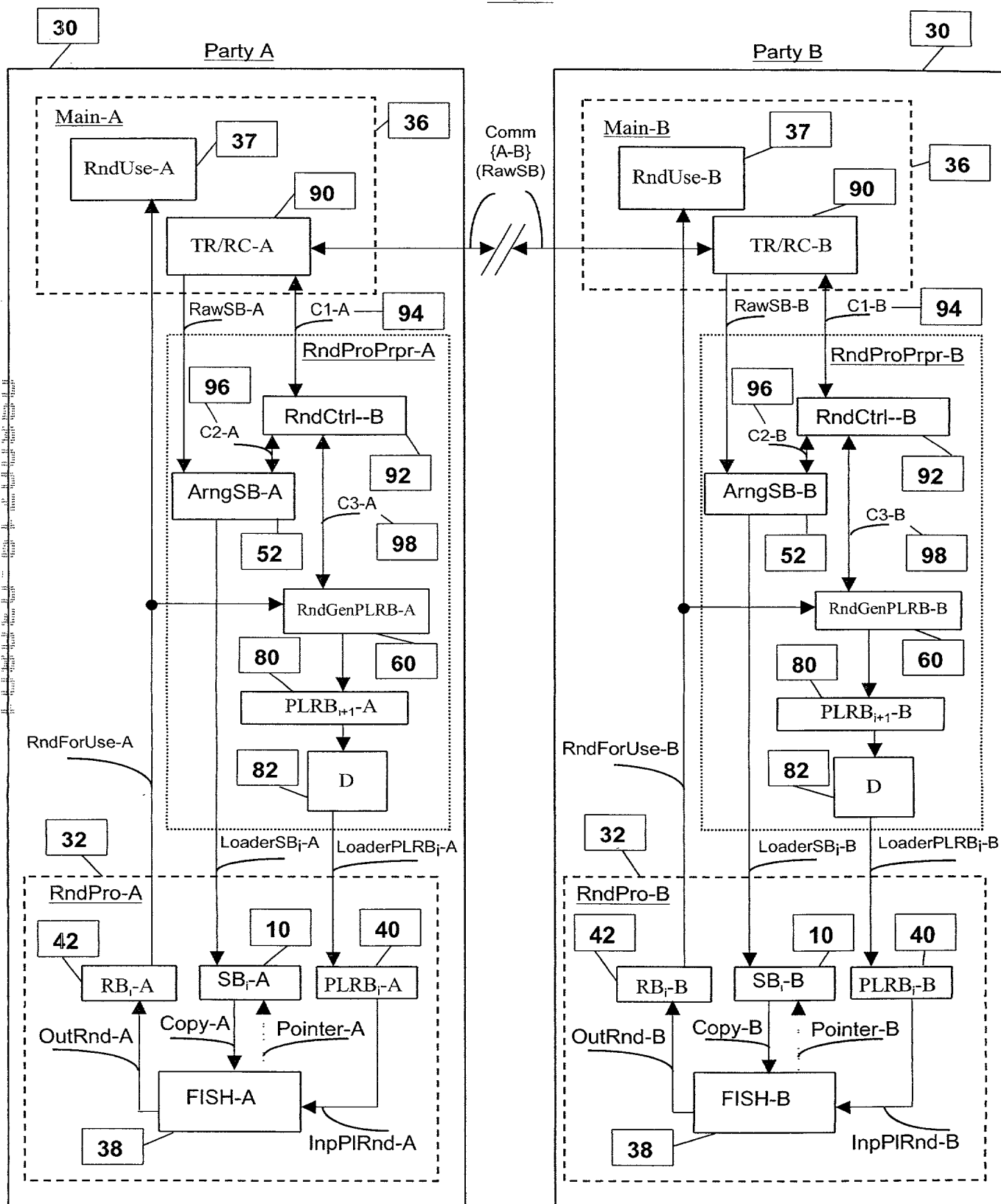


FIG. 13

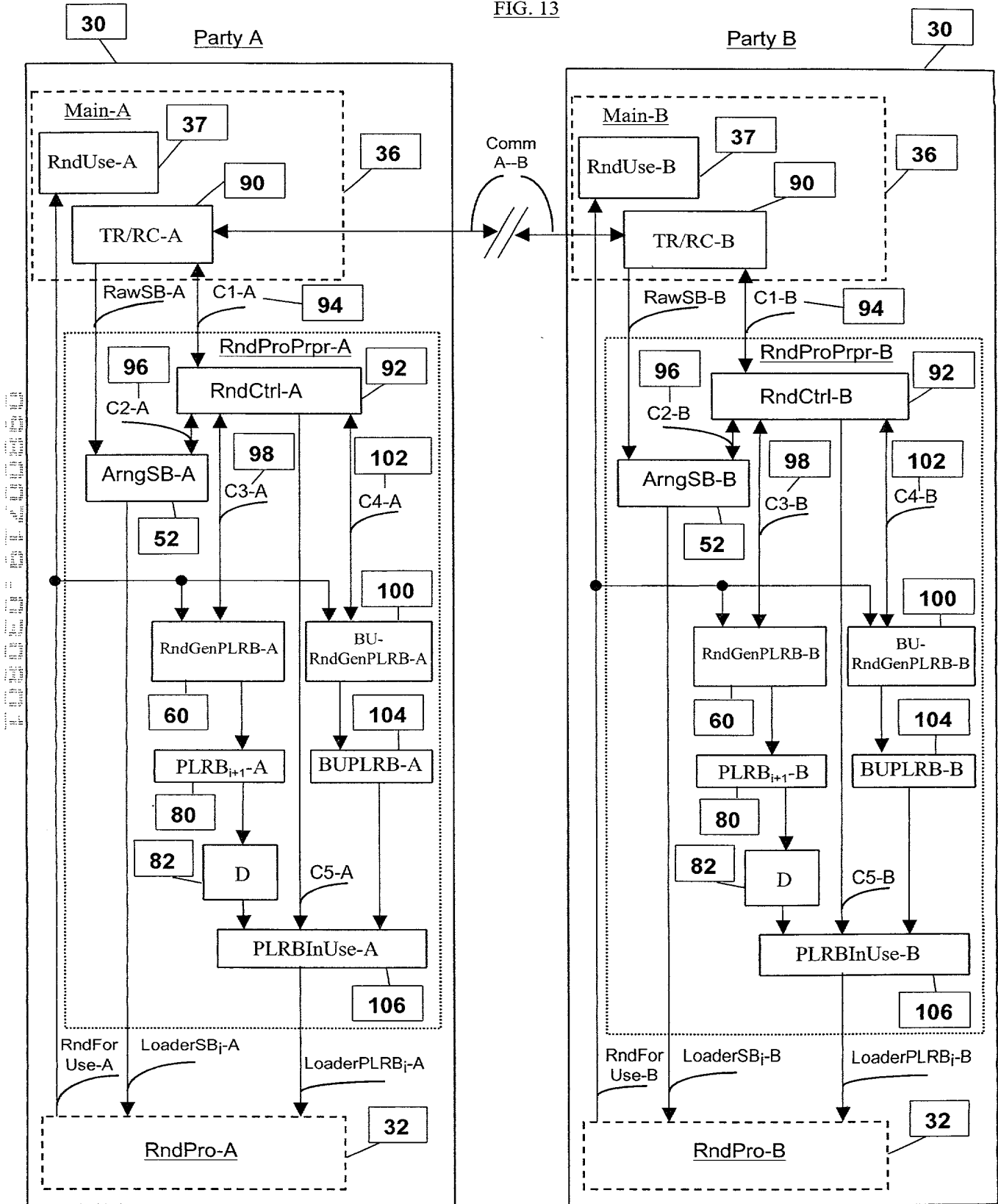


FIG. 14

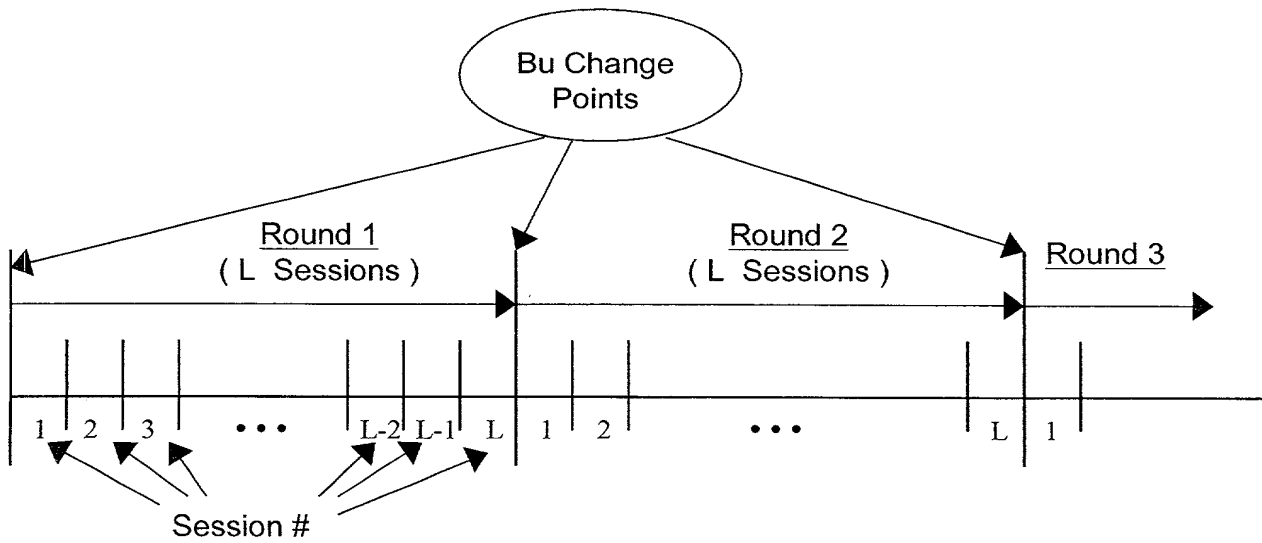


FIG. 15

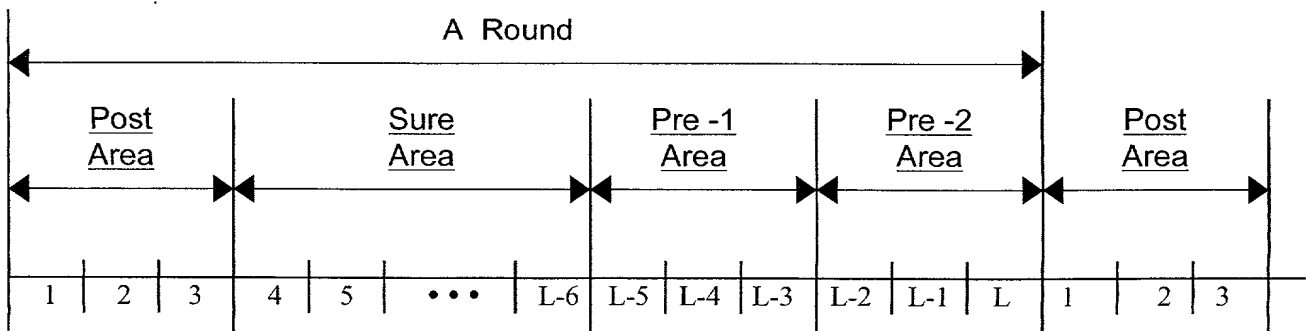


FIG. 16

Area	BU in Memory	Dominant		Slave	
		Control Snt	BU Use	Control Rcv.	BU Use
Sure	Current	Curr	Current	N.M	Current
Pre-1	Current	Curr	Current	Curr	Current
				Nxt	Next1
Pre-2	Current	Nxt	Next1	Curr	Current
				Nxt	Next1
Post	Next	Nxt	Next	N.M	Next